

# Scicos-HDL

Zhangdong&Kangcai 2009.03  
From China

<http://scicoshdl.sourceforge.net>

<http://www.scilab.org.cn/scicoshdl/index>

# 1/12 About SystemC

- SystemC is a C++ class library and a methodology that you can use to effectively create a cycle-accurate model of software algorithms, hardware architecture, and interfaces of your SoC (System On a Chip) and system-level designs.
- 
- You can use SystemC and standard C++ development tools to create a system-level model, quickly simulate to validate and optimize the design, explore various algorithms, and provide the hardware and software development team with an executable specification of the system.

## 2/12 About Scicos-HDL

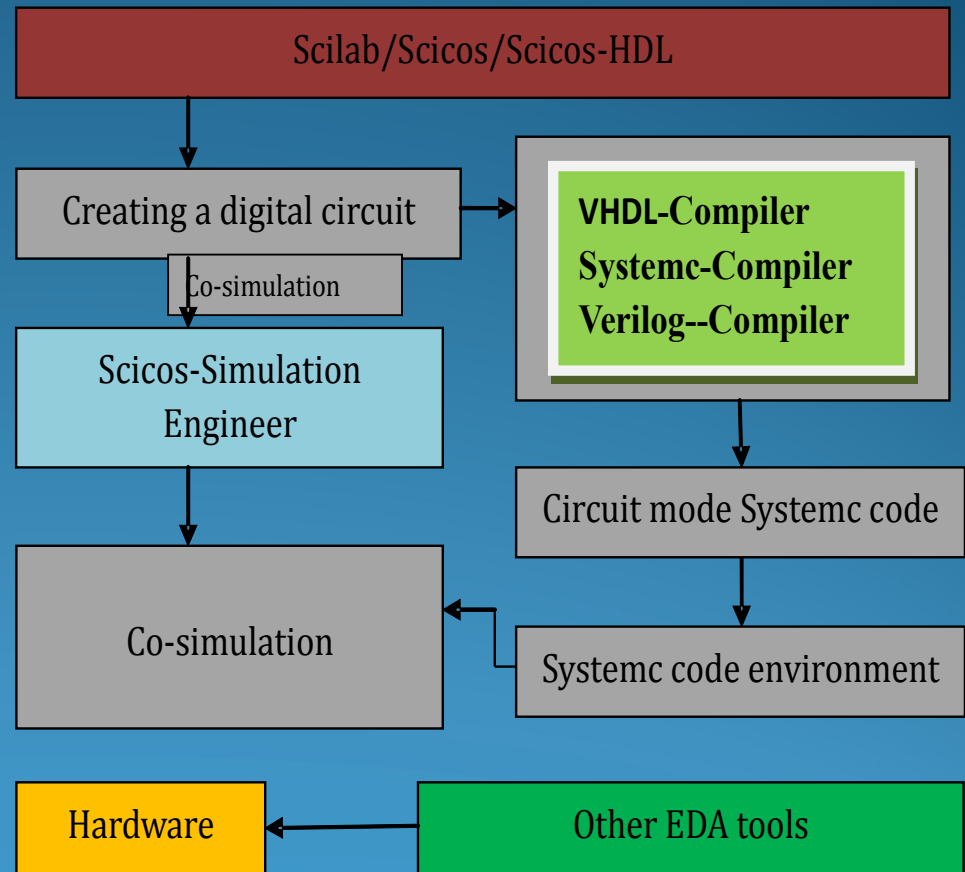
- Scicos-HDL is a toolbox based on Scicos and SystemC, its main function is to generate Systemc code from Scicos model, and it supports co-simulation with the original blocks of Scicos and Scicos-HDL blocks.
- 
- Scicos-HDL links Scicos with hardware circuit design and simulate in SystemC code. Comparing to Scicos-HDL, the simulation engine of Scicos-HDL is standard C++ language and SystemC library, this toolbox is more efficient.

# 3/12 Scicos-HDL Features

- Links SCILAB/SCICOS with SystemC library
- Automatically generates SystemC code
- Automatically generates a vcproject
- The new simulation engine of Scicos-HDL uses compiled language, more efficient than Scicos itself.
- Supports SystemC, VHDL and VERILOG.
- Scicos hardware-acceleration function: the model file designed by Scicos-HDL can be compiled and downloaded to FPGA to run. Users can control which part running in FGPA and which part running in computer, so Scicos can use the software-hardware co-simulation.

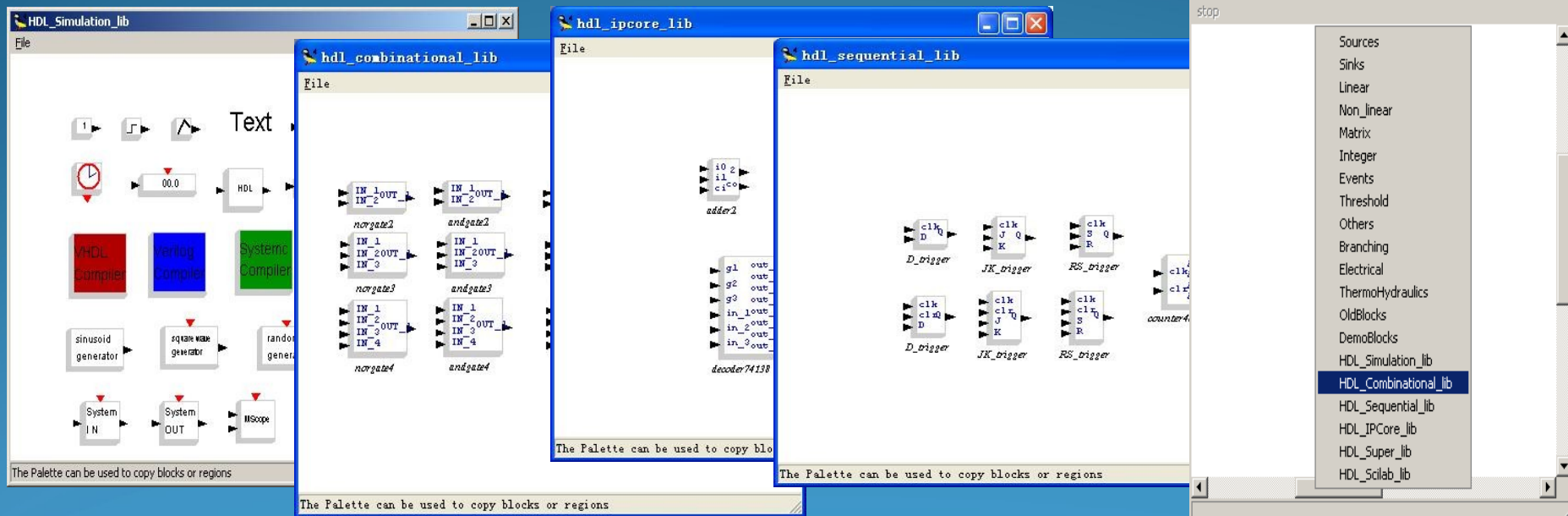
# 4/12 Design Flow

- Systemc-Compiler will generate the Systemc code of circuit and then start Scicos simulation engine and meanwhile start the Systemc environment to compile and run the whole mode project.



# 5/12 Install

- First , you should install Scilab, both in windows or Linux OS;
- Download the newest release of Scicos- HDL from here:
- <http://scicoshdl.sourceforge.net/>
- Ref. Scicos-HDL.pdf including in the package.



Digital system design basic library

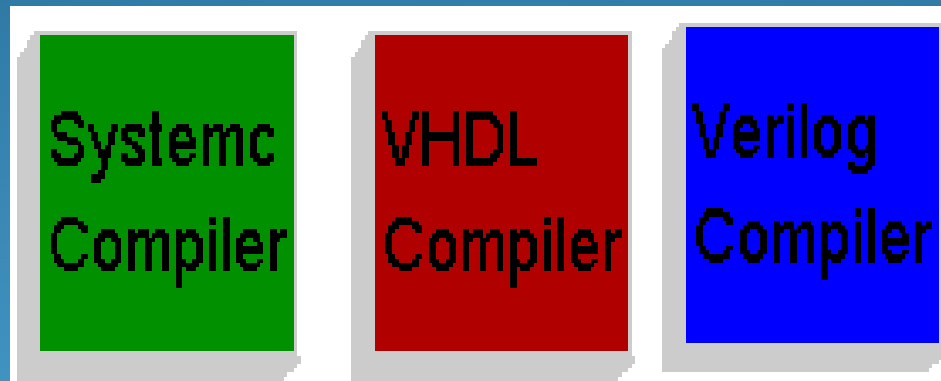
Combinational logic library

Sequential logic library

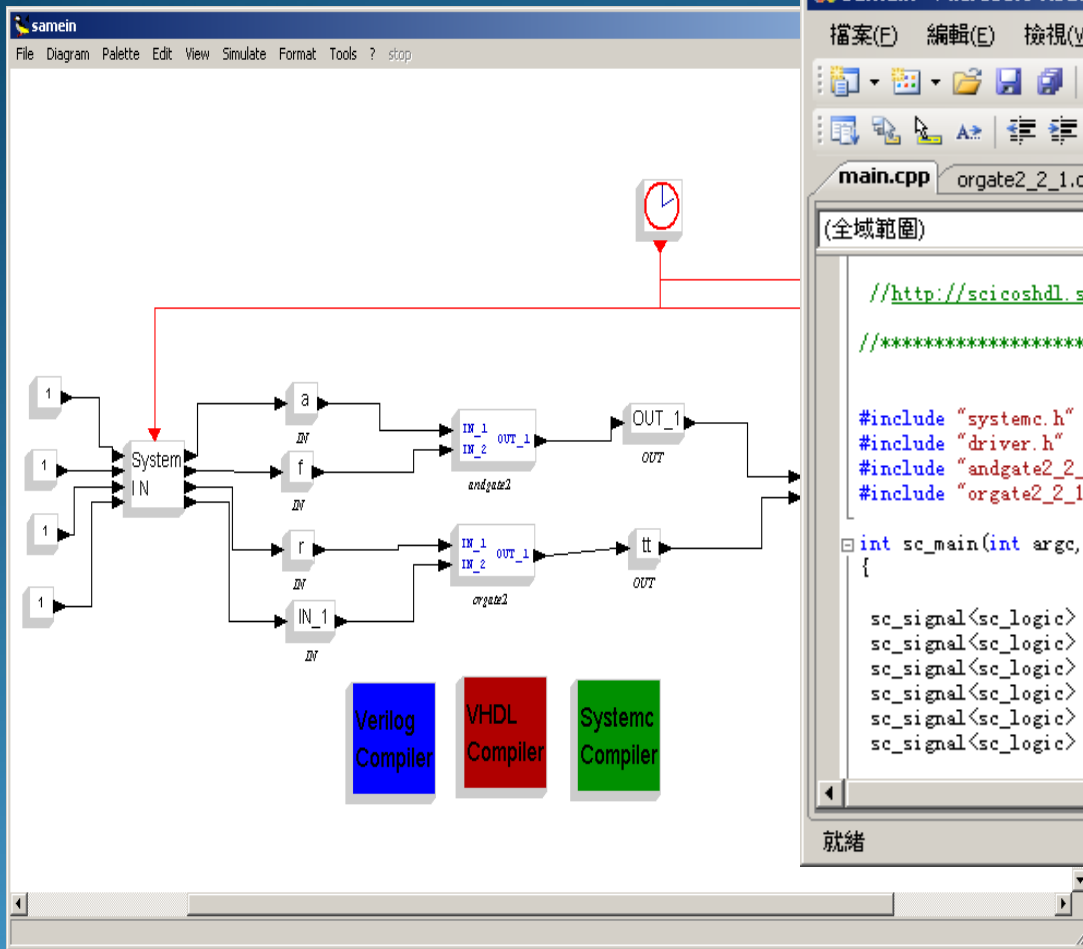
IP core library

# 6/12 How to use Scicos-HDL

- All the using steps are as the same as the steps of Scicos, both for modeling and simulation;
- Just use the Scicos-HDL Compiler to generate HDL code;



# 7/12 Examples



The screenshot shows Microsoft Visual Studio with the 'samein' project open. The 'main.cpp' file is selected, showing the following code:

```
//http://scicoshdl.sourceforge.net
//*****

#include "systemc.h"
#include "driver.h"
#include "andgate2_2_1.h"
#include "orgate2_2_1.h"

int sc_main(int argc, char* argv[])
{
    sc_signal<sc_logic> sciSig_f_11;
    sc_signal<sc_logic> sciSig_a_12;
    sc_signal<sc_logic> sciSig_OUT_1_13;
    sc_signal<sc_logic> sciSig_IN_1_9;
    sc_signal<sc_logic> sciSig_r_10;
    sc_signal<sc_logic> sciSig_tt_14;
```

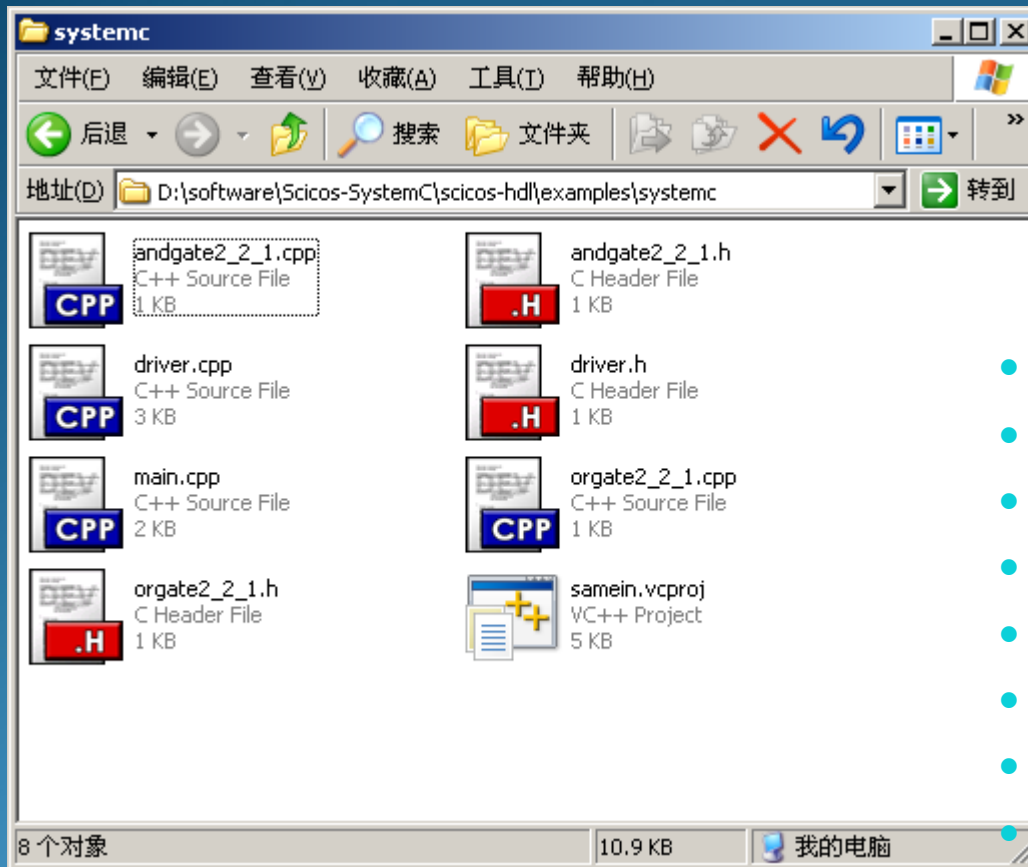
The status bar at the bottom indicates '就绪' (Ready), '第 16 行' (Line 16), '第 25 欄' (Column 25), '字元 25' (Character 25), and 'INS'.

Scicos Model

Systemc Codes in VS2008



# 8/12 SystemC code file generated



- File Structure

- files generated by Scicos-HDL

- samein.vcproj ----- project file

- main.cpp ----- main function

- andgate2\_2\_1.h ----- and gate

- driver.h ----- simulation file

- orgate2\_2\_1.h ----- or gate

- andgate2\_2\_1.cpp -- and gate

- driver.cpp ----- simulation file

- orgate2\_2\_1.cpp ---- or gate

# 9/12 Co-Simulation

The screenshot displays a co-simulation environment with the following components:

- Code Editor:** Shows the `main.cpp` file with C++ code for system instantiation. The code includes headers for `systemc`, `driver`, `andgate2`, and `orgate2`. It defines a `sc_main` function that instantiates a `System` block and connects it to `andgate2` and `orgate2` blocks.
- Block Diagram:** A schematic diagram showing a `System` block with an `IN` port. This block is connected to two `andgate2` blocks and one `orgate2` block. The `andgate2` blocks have inputs `a`, `f`, and `r`, and outputs `IN_1` and `OUT_1`. The `orgate2` block has inputs `IN_1` and `IN_2`, and output `OUT_1`.
- Scilab Graphic (20017):** A plot window showing a signal waveform. The y-axis ranges from -15 to 15, and the x-axis shows time in ns. The signal is a square wave that transitions from 0 to 1111 at approximately 2437 ns.
- Terminal Window:** Shows the output of the simulation, displaying a sequence of input and output values over time. The output is consistently 1111 for all input transitions.

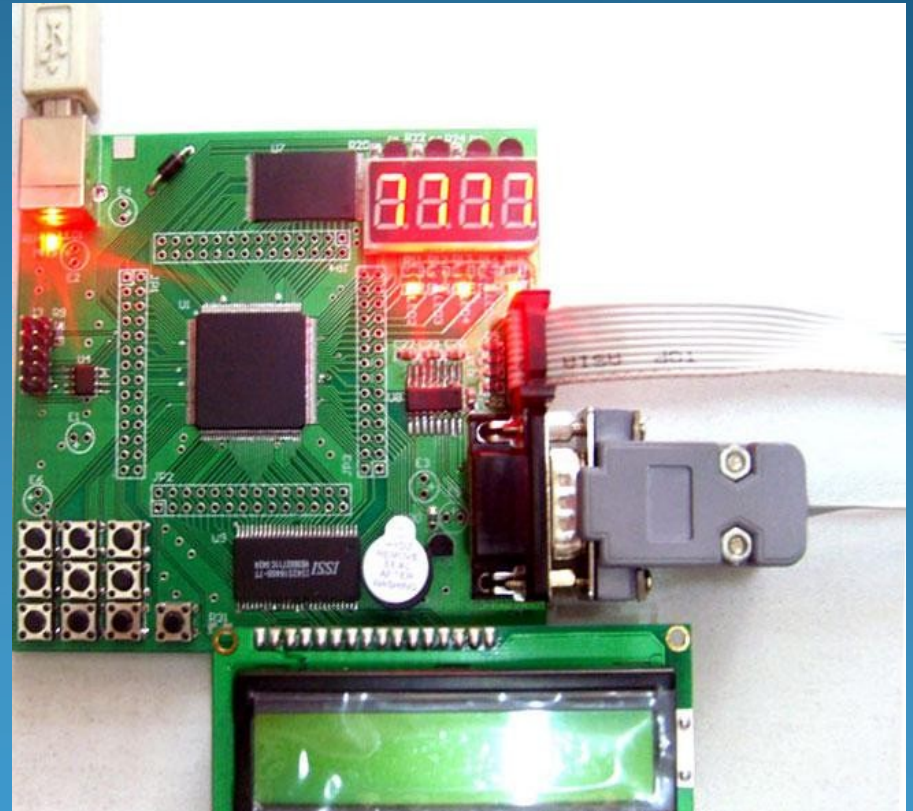
At the bottom of the code editor, there are three colored boxes representing the compilers used in the co-simulation:

- Verilog Compiler (Blue box)
- VHDL Compiler (Red box)
- Sys Comp (Green box)

The status bar at the bottom indicates the current line and column: 第 16 行 第 25 欄 字元 25.

# 10/12 Hardware-acceleration

- function: the model file designed by Scicos-HDL can be compiled and downloaded to FPGA to run.
- Users can control which part running in FGPA and which part running in computer, so Scicos can use the software-hardware co-simulation.



Web Site: <http://scicoshdl.sourceforge.net/>  
<http://www.scilab.org.cn/scicoshdl/index>

# 11 Meaning

Project Email: [scicoshdl@gmail.com](mailto:scicoshdl@gmail.com)

- ◆ Try out best to make Scicos-HDL as useful tool for the engineers;
- ◆ Enable Scicos automatically generate standard C++ codes
- ◆ Enable Scicos support SystemC hardware description block
- ◆ Enable Scicos use software–hardware co-simulation

# 12 Main Application

- ◆ High Performance Scientific Computing area
- ◆ FPGA application design and simulation area
- ◆ ... ..

Thank you

Zhangdong&Kangcai 2008.11

From China

END